REMARKS

Reconsideration of this application, in view of the foregoing amendments and the following remarks, is respectfully requested.

Claims 1-25 were pending for consideration in this application. By the foregoing amendment, Applicant has amended Claim 10. Claims 1-25 remain pending.

Claims 10-12 were rejected by the Examiner under 35 USC 101 as being directed to non-statutory subject matter. Applicant has herein amended independent Claim 10 to recite "executing … by a processor" to make it clear that this method is performed by a machine, and is therefore statutory subject matter. Claims 11-12 depend on Claim 10 and are therefore also directed to statutory subject matter. Applicant requests withdrawal of this rejection. Since the Examiner has asserted no other rejections against Claims 10-12, Applicant assumes Claims 10-12 are now allowable.

Claims 1-5, 13-17, and 22-25 are rejected by the Examiner under 35 U.S.C. 103(a) as being unpatentable over Magoshi (patent No. 6,988,187) in view of Kusiak (patent No. 5,434,986). Claims 6-9,18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Magoshi and Kusiak as applied to claims 1-5,13-17, and further in view of Catherwood (patent application publication No. 2003/0061464).

Catherwood illustrates a problem that is solved by Applicant's novel test and skip instruction. In Catherwood, over fifteen branch instructions are illustrated, see pages 52-72. Each includes an opcode and a sixteen bit offset value that is used by an address generator to determine a branch address. No other operands or test conditions are included in the instruction. In order to specify a particular test condition, a particular opcode is selected. Conversely, Applicant's skip instruction has no need for an offset field, therefore Applicant's test and skip instruction can include "a first register reference

and a second register reference and causes the processor to compare a first value comprising the register value stored in a register corresponding to the first register reference and a second value associated with the second register reference and to execute or not execute a subsequent instruction that follows the test and skip instruction based on the comparison" as recited in Applicant's Claim 1 and similarly in independent Claims 10, 13, and 22. This allows a single test and skip opcode to be used while specifying a wide range of test conditions, as recited in Applicant's Claims 1-25. Since Catherwood's branch instructions do not include any operand fields other than the sixteen bit address offset and Catherwood has no teaching or suggestion of a test and skip instruction that includes references to two registers, or even to one register, or to a condition specified **in** the test and skip instruction, Applicant requests withdrawal of rejections of Claims 6-9, 18-21 based on Catherwood.

The Examiner admits that Magoshi has no teaching regarding registers being used during execution of a skip instruction. The Examiner characterizes Kusiak as teaching

> this limitation (e.g., see fig. 4, element 100 is a general register stack which is coupled to arithmetic logic unit 102) [in figures 10,11, and 12 when a skip instruction is encountered a test of whether the register reference values are equal is made for determining whether to skip a next instruction, e.g., see col. 11, lines 20-65].

Applicant respectfully disagrees with this characterization of Kusiak. Magoshi teaches that a skip instruction may be a branch instruction with "a relatively near forward target address." (Col 6, lines 21-28) Similarly, Kusiak teaches "…. skip instruction represents a special case of conditional branch instructions …" (Col. 11, lines 30-36). Further, Kusiak teaches "the next executed instruction depending upon whether the skip condition is or is not met." (Col 11, lines 32-42) However, Applicant finds no teaching or suggestion in either Kusiak or in Magoshi alone or together of Applicant's novel method and logic for determining the skip condition as claimed in Applicant's independent Claims 1, 10, 13, and 22. Recall that in Catherwood each of over fifteen different conditional branch instructions include only an opcode and an address offset parameter, and presumably the conditional branch instructions of Kusiak and Magoshi are similar since they have no

additional teachings. For example, Applicant's Claim 1 recites: "…a test and skip instruction …that **includes** a first register reference and a second register reference and causes the processor to compare a first value comprising the register value stored in a register corresponding to the first register reference and a second value associated with the second register reference and to execute or not execute a subsequent instruction that follows the test and skip instruction based on the comparison". Applicant finds no teaching or suggestion in Magoshi or in Kusiak of a skip instruction that uses two registers to determine a skip condition. Independent Claims 1, 10, 13 and 22 are clearly allowable over Magoshi and Kusiak in any combination. Applicant respectfully requests withdrawal of this rejection.

Claim 10 further recites: "examining a bit in the test and skip instruction; comparing contents of a first register to contents of a second register if the bit is in a first state; or comparing the contents of the first register to contents of a non-register location if the bit is in a second state;…" Neither Magoshi or Kusiak in any combination suggest such a method for determining a skip condition.

Claims 2-9, 11-12, 14-21 and 23-25 depend directly or ultimately on allowable base claims and are therefore allowable for this reason and by virtue of their further distinctive recitations. For example, for comparison of the two values recited in Claim 1, Claim 2, and similarly Claim 14, recites: "…wherein the second value comprises a register value stored in the second register reference." The Examiner points to Kusiak, Col 2, lines 20-65, which is a long list of other references which seem to relate to branch prediction and branch address calculation. The Examiner has failed to point out anything suggesting using a register value stored in a second register referred to by the test and skip instruction for the skip comparison. Claims 2 and 14 are therefore allowable over the cited references for this additional reason.

Claim 3, and similarly Claims 15 and 24, recites "the second value is stored in the memory." As explained above, neither reference suggests determination of a skip

condition by comparing a register value to a value stored in memory, where the test and skip instruction includes a reference to the memory location. The Examiner points to Kusiak Col 10, line 24-45, which describes nothing more than branch prediction and instruction prefetching. However, Applicant sees nothing suggesting a test and skip instruction that includes a first register reference and a second register reference as recited in Claim 1 and wherein the second value associated with the second register is stored in memory. Claims 3 and 15 are therefore allowable over the cited references for this additional reason.

Claim 5, and similarly Claim 17, recites: "…wherein the pointer is computed by adding the value from the second register reference to a register value from another register." Applicant respectfully points out this pointer is used to determine a value to be used in the comparison of Claim 1 to determine if the following instruction will be skipped. The Examiner points to Kusiak, Col 7, lines 15-55, which describes an address generator that calculates a jump address, which has nothing to do with determining a value to be used in the comparison of Claim 1 to determine if the following instruction will be skipped. Claims 5 and 17 are therefore allowable over the cited references for this additional reason.

Claim 7, and similarly 18, recites: "…wherein the comparison includes a condition that is specified in the test and skip instruction. As discussed above, neither Catherwood, Kusiak, nor Magoshi suggest a test and skip instruction in which the condition is specified **in** the test and skip instruction. Catherwood uses separate opcodes to imply each condition used by the more than fifteen conditional branch instructions, but has no suggestion of including a field **in** the conditional branch instruction to specify the condition.

Applicant reserves comment on the other references not relied on by the Examiner.

Applicant believes this application and the claims herein to be in a condition for allowance and respectfully requests that the Examiner allow this application to pass to the issue branch.

Applicant believes that no additional fee is due at this time; however, please charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 relating to this matter to Deposit Account Number 20-0668, for Texas Instruments Incorporated.

Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

Respectfully submitted,

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